REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-33 in the application. The Examiner has indicated that Claims 9, 20 and 31 include allowable subject matter. The Applicants believe that each of the present pending claims is allowable.

In the present response, the Applicants have amended Claims 1, 4-5, 9, 12, 15-16, 20, 23, 26-27 and 31 and have added Claims 34-36. Support for the new claims can be found in paragraph 30 on pages 12-13 and in Figure 2 of the original specification. No claims have been canceled in the present response. Accordingly, Claims 1-7, 9-18, 20-29 and 31-36 are currently pending in the application.

I. Rejection of Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103

The Examiner has rejected Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103(a) as being unpatentable over of U.S. Patent No. 6,552,619 to Shastri in view of U.S. Patent 5,651,031 to Ishizu. The Applicants respectfully disagree.

Shastri is directed to a multi-channel clock recovery circuit where multiple channels use a common voltage controlled oscillator. (*See* column 1, lines 8-11.) Shastri discloses a mult-channel clock recovery circuit 1 that includes a plurality of clock recovery circuits that each provide clock signals to a corresponding de-serializer circuit 8. (*See* column 5, lines 10-18 and Figure 1.) Shastri does not teach or suggest, however, a plurality of channel-specific receivers coupled to a central frequency synthesizer with each of the plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal. On the contrary, Shastri concentrates on clock recovery and

teaches the de-serializer circuit 8 employs clock signals from a corresponding clock recovery circuit to convert input data into parallel data. (*See* column 5, lines 18-23.) The Applicants do not find where Shastri provides any teaching or suggestion of the de-serializer circuit 8 having integrators and latches configured to perform demultiplexing. Thus, for at least these reasons, Shastri does not teach or suggest each of a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23.

Ishizu has not been cited to cure the above deficiency of Shastri. Additionally, the Applicants do not find where Ishizu cures the above deficiency of Shastri. On the contrary, Ishizu is directed to clock recovery circuits of demodulators. (*See* column 1, lines 14-15.) Ishizu discloses using integrators in a clock phase detector of the clock recovery circuits (*see* column 1, line 47 to column 2, line 4 and Figure 26) but does not teach or suggest employing integrators for demultiplexing a data signal. Thus, Ishizu does not teach or suggest each of a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23.

The cited combination, therefore, of Shastri and Ishizu does not teach or suggest each of a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23. As such, the cited combination does not provide a *prima facie* case of obviousness of independent Claims 1, 12 and 23 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of independent Claims 1, 12

and 23 and Claims dependent thereon and allow issuance of Claims 1-3, 10, 12-14, 21, 23-25 and 32.

Furthermore, one skilled in the art would not be motivated to combine the analog integrators disclosed in Ishizu with the teachings of Shastri to arrive at the present invention since Shastri is directed to a deserializer that utilizes all digital sampling of a serial data signal to convert the serial data to parallel data. (*See* Figure 1 of Shastri.)

II. Rejection of Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103

The Examiner has rejected dependent Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103(a) as being unpatentable over Shastri in view of Ishizu and in further view of other references. The other references have not been cited to teach or suggest a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23. Instead, these references have been cited to teach the subject matter of specific dependent claims listed above. Accordingly, the cited combination of Shastri, Ishizu with any of the other references does not teach or suggest each and every element of independent Claims 1, 12 and 23. As such, the cited combinations do not provide a *prima facie* case of obviousness of Claims 1, 12 and 23 and Claims dependent thereon. The cited combinations, therefore, do not render dependent Claims 4-7, 11, 15-22, 26-29 and 33 unpatentable and the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of dependent Claims 4-7, 11, 15-22, 26-29 and 33 and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-36.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to deposit account 08-2395.

Respectfully submitted,

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Dated: 11/4/05

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